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App Note 2351: DS31256 and DS3134 HDLC Controller Comparisons

This application note compares the differences between the DS3134 Chateau and DS31256 Envoy HDLC controllers. The most important difference is that all known DS3134 errata have been fixed in DS31256, and the DS31256 is both hardware and software backward compatible with the DS3134.

The table below summarizes the major differences between the DS3134 and the DS31256.

Table 1.

No.	Category	Register	DS3134 B2	DS31256 A2	DS31256 B2
1	Number of high-speed ports	--	2	3	3
2	Maximum throughput	--	104Mbps	132Mbps	132Mbps
3	Non-DWORD-aligned buffer support	--	Full	None	Tx side only
4	Arbitration Priority Reversals	MC[13:12]	See detail descriptions below		
		MC[15:14]			
5	Revision ID	MRID[15:8]	0x01	0xC1	0xB1
6	PCI Revision ID, Function 0	PRCC0[7:0]	0x00	0x00	0x01
7	PCI Revision ID, Function 1	PRCC1[7:0]	0x00	0x00	0x01
8	JTAG IDCODE Device	--	0x0006	0x001A	0x001A
9	JTAG IDCODE Revision	--	0x0	0x0	0x1

Detailed Descriptions for Items 1 Through 4

1) Ports 0, 1, and 2 all support high-speed unchannelized mode in the DS31256. In the DS3134, only ports 0 and 1 support high-speed unchannelized mode. Refer to the DS31256 data sheet for details.

2) The maximum full-duplex throughput of the DS31256 device is 132Mbps, while the maximum throughput of the DS3134 is 104Mbps. The DS31256 supports 60 T1 or 64 E1 lines, whereas the DS3134 only supports from 32 to 40 T1/E1 lines, depending on configuration. The DS31256 supports oversubscription, where the sum of the clock rate on all ports on a device can exceed the throughput capability of the device so long as the sum of the line utilizations of all active ports never exceeds the throughput capability of the device. An active port is one that is currently transmitting or receiving data. Transmit throughput and receive throughput are calculated independently. For example, the device can support 16 unchannelized ports operating at a clock frequency of 10MHz (160Mbps) as long as no more than 13 of them (130Mbps) are ever simultaneously at 100% utilization at any given time. Oversubscription is not possible on the DS3134 since idle ports are clocked, but with no traffic can also consume device throughput.

3) The DS31256 B2 has no restrictions on the transmit side, but has the following restrictions on the location and size of receive-side buffers in host memory. Refer to the DS31256 A2 Errata (www.maxim-ic.com/errata) for details.

- All Rx buffers must start on DWORD-aligned addresses.
- Rx buffers must have a size in bytes that is a multiple of 4.
- Rx buffer offsets are no longer supported - Rx DMA configuration RAM dword2[6:3].

The DS3134 does not have these restrictions, so this could create a backward compatibility issue. Since the transmit side of the DS31256 B2 revision can handle non-DWORD-aligned addresses, header modifications may be performed as simply and directly as with the DS3134.

4) Arbitration Priority Reverals
The programmable Tx and Rx FIFO arbitration scheme modes in DS31256 are different from the DS3134. Selection of the Tx and Rx FIFO arbitration scheme in the DS31256 is defined as follows in the MC register:

MC[13:12] : Receive FIFO Priority Control

00 = All HDLC channels are serviced round robin.

01 = HDLC Channels 1 through 3 are priority decoded in sequence with Channel 1 having the highest priority. Other channels are serviced round robin if channels 1 through 3 do not require servicing.

10 = HDLC Channels 16 through 1 are priority decoded in sequence with Channel 16 having the highest priority. Other channels are serviced round robin if Channels 16 through 1 do not require servicing.

11 = HDLC Channels 64 through 1 are priority decoded in sequence with Channel 64 having the highest priority. Other channels are serviced round robin if Channels 64

through 1 do not require servicing.

MC[15:14] : Transmit FIFO Priority Control

00 = All HDLC channels are serviced round robin.

01 = HDLC Channels 1 through 3 are priority decoded in sequence with channel 1 having the highest priority. Other channels are serviced round robin if channels 1 through 3 do not require servicing.

10 = HDLC Channels 16 through 1 are priority decoded in sequence with channel 16 having the highest priority. Other channels are serviced round robin if channels 16 through 1 do not require servicing.

11 = HDLC Channels 64 through 1 are priority decoded in sequence with channel 64 having the highest priority. Other channels are serviced round robin if channels 64 through 1 do not require servicing.

If the '00 mode of the Transmit FIFO Priority Control is used on both the Transmit and Receive sides, the DS31256 is backward compatible with DS3134. In mode '01, the third high speed port in DS31256 becomes a member of the first group, where it was a low speed round robin port on DS3134. Otherwise, modes '10 and '11 require a reversal of the channel assignments made in the DS31256 software to exactly match arbitration behavior to DS3134. Example for mode '10 : Channel 1 and channel 16 assignments are reversed, channels 2 and 15 are reversed, etc.

More Information

DS3134: QuickView -- Full (PDF) Data Sheet -- Free Samples